Comparison of Active MMIC Recursive Filter for Communication Systems in SiGe BiCMOS and ED02AH

Pejman Langari

***Abstract*—The aim of this study is to compare BiCMOS and ED02AH technologies in active MMIC recursive filters. These filters are designed using monolithic microwave integrated circuit (MMIC) technology. The central frequency of them is 4GHz. In this article we represent comparison of analytical and computer-simulated result in ADS software using 0.35µm SiGe BiCMOS and 0.2µm ED02AH process technologies.**

***Index Terms*—Active recursive filter, all-pass cell, time delay, MMIC.**

I. Introduction

By increasing mobile communication, filters have to be miniaturized so that they would be integrated into MMIC modules along with other microwave action like amplifiers, mixers or oscillators. Active filters represented an attractive solution while conventional passive filters require much of space as well as displaying high losses. Current fulfillment of recursive filters has revealed that a given signal flow graph could be translated into any numbers of physical design [1]. This research deals with active recursive filters in 0.35µm SiGe BiCMOS and 0.2µm ED02AH technologies [1].

II. Simplified Recursive Filter

The transfer function of a simplified recursive filter is given by:

$$H(j\omega) = \frac{a_0}{1 + b_1 e^{-2i\pi f \tau}} \quad (1)$$

Our approach, qualified cellular, consists of synthesizing a transfer function in association with poles and zeros which could be characterized individually. It means that instead of studying a complex recursive structure with transfer functions, we can study simplified recursive structures. The synthesis of the filter consists of determination of coefficients a_0 and b_1 and time delay τ.

III. Electrical Topology

The Electrical topology of simplified recursive filter is given in Fig. 1 [2]. The filter works in the microwave range, and is characterized by its S-parameters. Furthermore, in the vicinity of the central frequency, the filter should be conformed both at input and output (S11=S22=0). The different gain stages (A_0, A, A_1, B) and time delay are described as bellow. The effect of Gain stage B is considered in time delay cell, so stage *B* is eliminated in structure of filter.

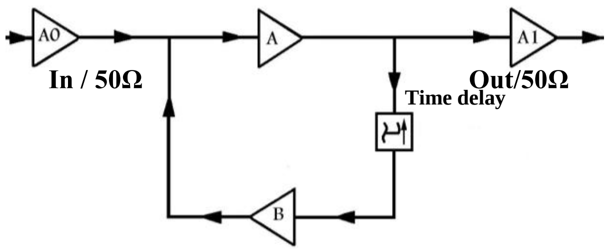

Fig. 1. Electrical topology of simplified recursive filter.

IV. Comparison of Gain Stage in both BiCMOS and ED02AH

The cell A_0 must have input impedance equal to 50Ω and high output impedance. The input impedance condition is fulfilled with a common base transistor and common emitter transistor and it permits us to obtain high output impedance and the desired gain in BiCMOS technology. This features are shown in ED02AH technology whit both common gait and common source transistor. The biasing of each structure is realized with active load (see Fig. 2).

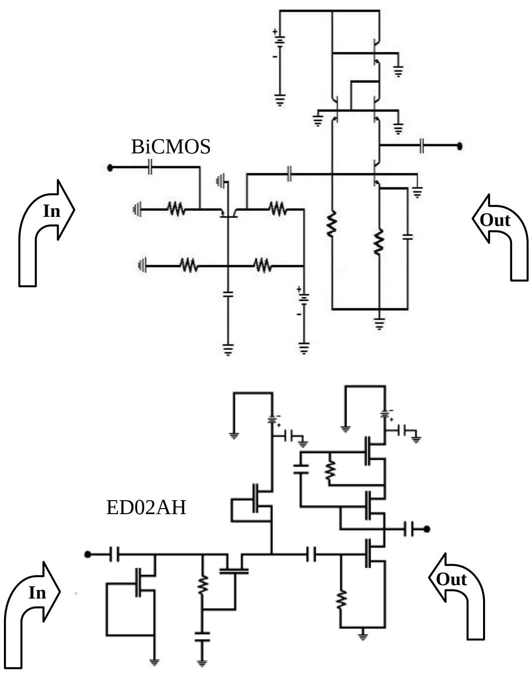

Fig. 2. Schematic diagram of the amplification A0 in BiCMOS and ED02AH .

Manuscript received December 7, 2012; revised October 1, 2013.

Pejman Langari is with the Electrical Engineering department of Islamic Azad University of Bojnord, Bojnord, Iran (e-mail: pejman_langari@bojnourdiau.ac.ir).

DOI: 10.7763/IJMLC.2013.V3.347

Current voltage converter cell A must have very small input impedance compared to output impedance of cell A_0 and output impedance of the return chain B. The output impedance of cell A must be higher compared to the characteristic impedance Z_0 (50Ω) of the delay cell. Cell A is designed with a common base transistor in BiCMOS technology and common gait transistor in ED02AH technology. The biasing is with active load (see Fig. 3).

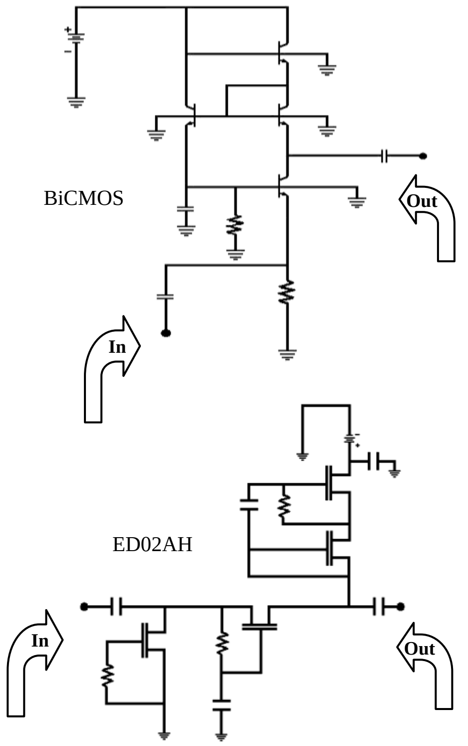

Fig. 3. Schematic diagram of the amplification A in BiCMOS and ED02AH.

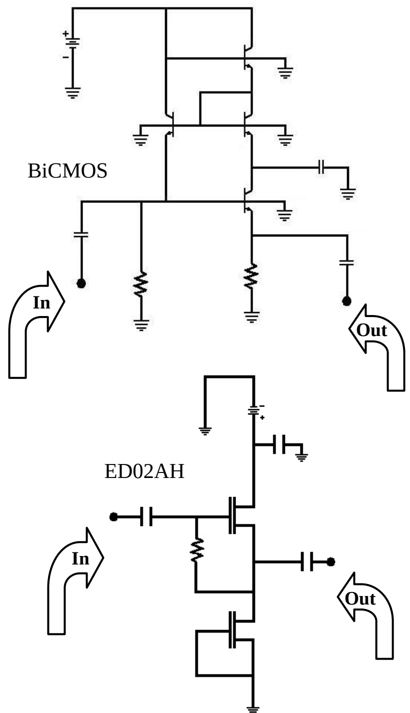

Fig. 4. Schematic diagram of the cell A1 in BiCMOS and ED02AH.

Cell A_1 must have very high input impedance in order not to charge the output and have output impedance equal to 50Ω. These two conditions are fulfilled with a common collector transistor in BiCMOS technology and a common drain transistor in ED02AH technology. The biasing of each common collector and common drain are realized with active load (see Fig. 4).

V. Active Time Delay Topology

A. All Pass Cell Topology

The phase shifter is designed with all pass cell bridge. Each of all pass cell generate 180° phase shift around the central frequency f_0 =4 GHz. A 360° phase shift and a considerable time delay are obtained by cascading two identical cells. We have simulated two identical cascaded all-pass cells around the central frequency f_0 =4 GHz. In order to have the same phase frequency as for an ideal time delay, we have optimized each elements of the cell. The power gain would be 0dB if the inductors which used in the circuit were ideal (see Fig. 5).

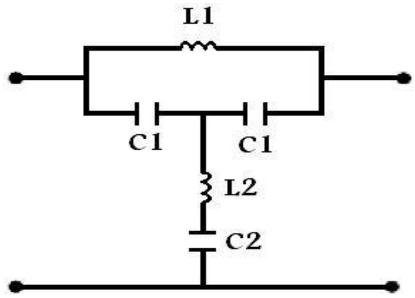

Fig. 5. Topology of an all-pass cell.

By using real inductor model, we notice an important gain drop, without any changes in the phase shift. According to these results, it is necessary to add an active compensation circuit for the inductor losses (see Fig. 6).

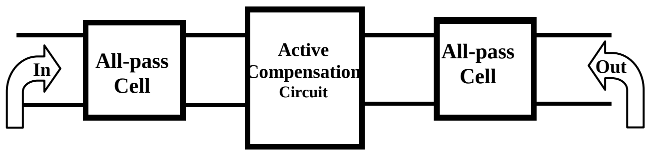

Fig. 6. Block diagram of two cascaded all-pass cells and the active Compensation.

VI. Compensation Circuit

The active compensation circuit is implemented with two common emitter stages in BiCMOS technology and two common source stages in ED02AH technology in cascade configuration with active loads. In compensation circuit, a common series-connected twoelements matching network is used. Both cascade transistors in each technology are inserted among the time delay cells [2]-[7].

VII. Time Delay Topology

The complete schematic of active monolithic microwave time delay of BiCMOS and ED02AH technologies are shown in Fig. 7. S21 and phase of S21 for each of BiCMOS and ED02AH are shown in Fig. 8. This time delay is fixing in

4GHz.

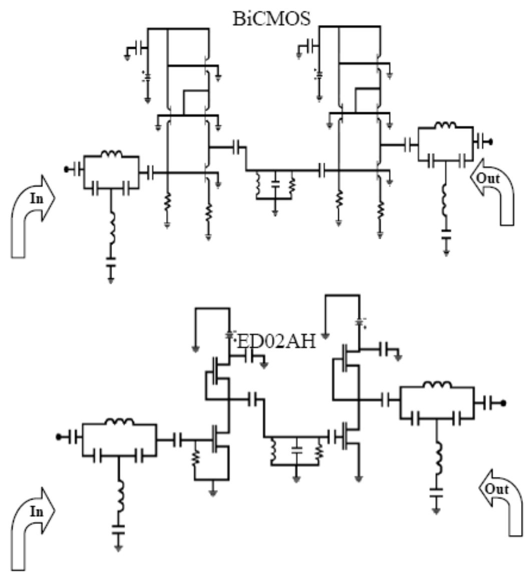

Fig. 7. Schematic of active MMIC time delay in BiCMOS and ED02AH.

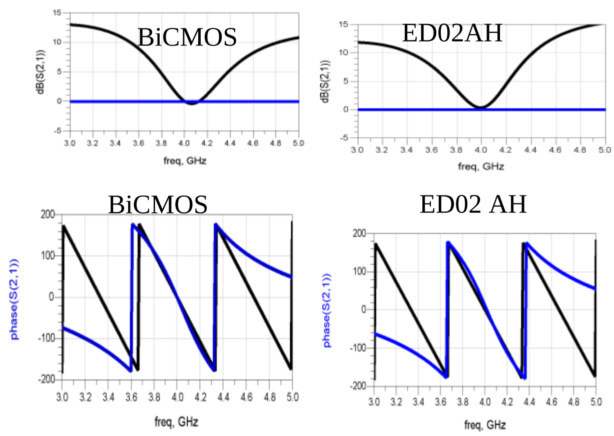

Fig. 8. Simulation results of two cascaded all-pass cells with losses in BiCMOS and ED02 AH technologies.

VIII. MMIC Recursive Filter Design

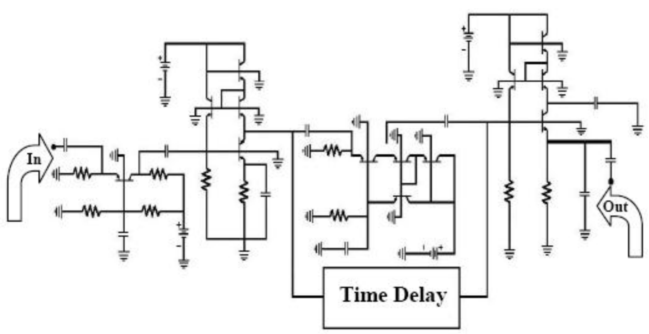

Fig. 9.1. MMIC Active Recursive Filter in BiCMOS technology.

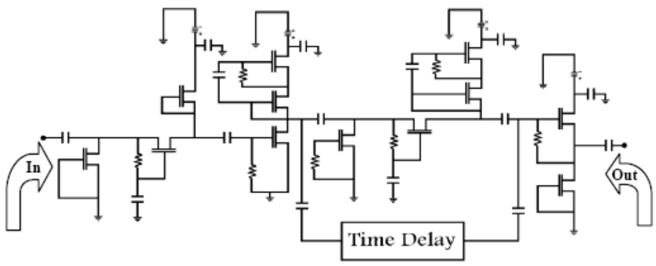

Fig. 9. 2. MMIC Active Recursive Filter in ED02 AH technology.

The active MMIC recursive filters for both structures are shown in Fig. 9. 1 and Fig. 9. 2. These filters may be compared to an ideal band pass active filter on an 800MHz bandwidth around a central frequency f_0 = 4 GHz. The gains S21 of these filters are shown in Fig. 10. The gain in BiCOMS is 14 dB and in ED02AH is 9dB. The quality of coefficient Q in BiCOMS is 85 and ED02AH is 50 and also input-output S11, S22 of BiCOMS is less than -20dB and ED02AH is less than -30dB (Fig. 11) [8]-[10].

We have studied the influence of technological parameter dispersion. The filters are not sensitive to parameter dispersion. The simulation of these filters with 5% tolerance for active and passive elements(R, C, L...) is shown in Fig. 12 and Fig. 13.

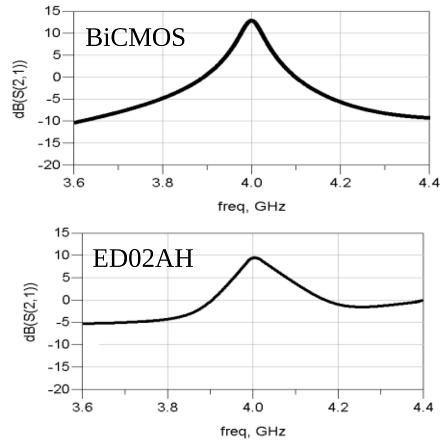

Fig. 10. S21 simulation of active recursive filter in both technologies.

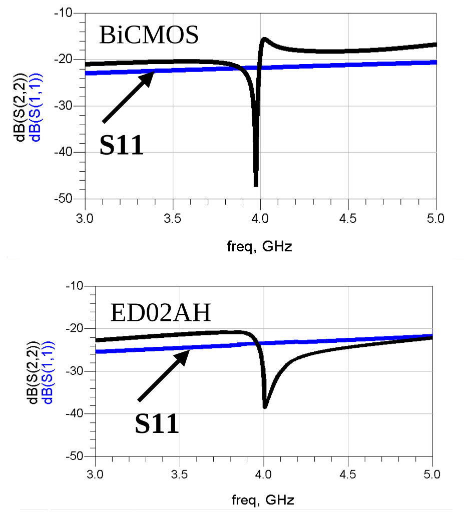

Fig. 11. S11 and S22 simulation of active recursive filter in both technologies.

The stability of these filters has been studied by Rolette coefficients (K). These coefficients are always greater than one between 1-10 GHz. The circuit power consumptions in BiCMOS are 27.4 mW and in ED02AH is 150-160 mW.

IX. Conclusion

The active MMIC recursive filters for both structures are shown in Fig. 9. 1 and Fig. 9. 2. These filters may be compared to an ideal band pass active filter on an 800MHz bandwidth around a central frequency f_0 = 4 GHz. The gains

S21 of these filters are shown in figure 10. The gain in BiCOMS is 14 dB and in ED02AH is 9dB. The quality of coefficient Q in BiCOMS is 85 and ED02AH is 50 and also input-output S11, S22 of BiCOMS is less than -20dB and ED02AH is less than -30dB (Fig. 11).

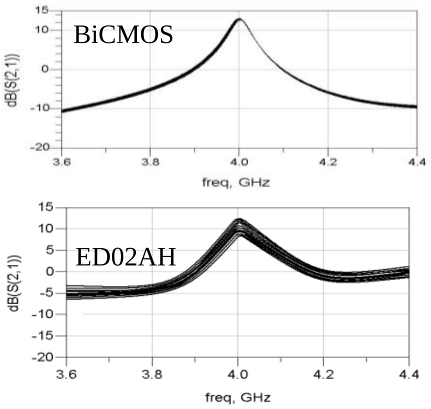

Fig. 12. S21simulation with 5% tolerance in both technologies.

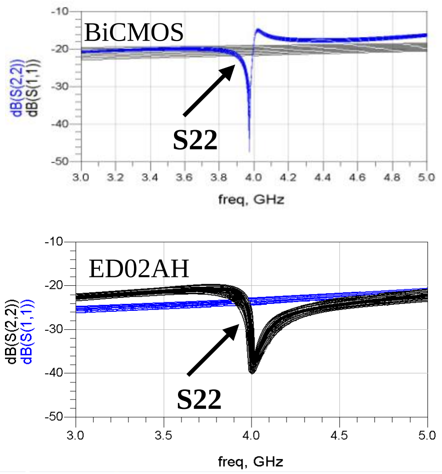

Fig. 13. S11 and S22 simulation with 5% tolerance in both technologies.

References

[1] M. J. Schindler and Y. Tajima, "A novel MMIC active filter with lumped and transversal elements," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 2148-2153, Dec. 1989.

[2] M. Dousti, B. Delacressoniere, F. Temcamani, and J. L. Gautier, *Active MMIC wideband Time Delay*, John Wiley & Sons, Microwave and Optical Technology Letters, 1997.

[3] L. Darcel, P. Dueme, R. Funck, and G. Alquie, " New MMIC approach for low noise high order active filters," *IEEE*, June 2005.

[4] A. L. Wolff, *Coplanar Microwave Integrated Circuits*, John Wiley, August 2006.

[5] H.-R. Ahn, *Asymmetric Passive Components in Microwave Integrated Circuits*, John Wiley, August 2006.

[6] S. Mikumo and Y. Yamamoto, "A band-pass filter based on the optically controllable S22 PARAMETER of a MESFET," vol. 2, no. 3, pp. 86-90, *IEICE Electronics Express*, February 2005.

[7] J. L. O. Cervantes, A. C. Chavez, D. V. B. Murthy, and H. L. Morales, "A wideband band pass filter with improved out-of-band performance," vol. 6, no. 16, pp. 1143-1147, *IEICE Electronics Express*, August 2009.

[8] P. Langari and M. Dousti, "A tunable active mmic recursive filter for communication systems in SiGe BiCMOS," *IEEE*, 2009.

[9] P. Langari, M. Pourakbar, M. Dousti, F. Temcamani, B. Dracressoniere, and J. L. Gautier, "A tunable active mmic time delay for communication systems in SiGe BICMOS technology," *IEEE*, 2008.

[10] M. Pourakbar, P. Langari, M. Dousti, F. Temcamani, B. Dracressoniere, and J. L. Gautier, "A 1.2-V single-stage, SiGe BiCMOS low-noise amplifier at 5.8GHz for wireless applications," *IEEE*, 2008.

P. Langari was born in Bojnourd, Iran at Feb. 20, 1980. He has got master of electronic major and he graduated from Dep. Of Electronics, Islamic Azad University (IAU), Science & Research Branch Tehran in 2006.