Parallel Processing Architecture for ECG Signal Analysis

Poorna Chandra Suraj B. N, Veena Hegde, and Abhishek Kumar Thakur

***Abstract*—Research in detecting QRS peaks in ECG signals has progressed to an acceptable extent and hence has gained adequate confidence with respect to the validity of the outputs produced. In view of the dynamics associated with ECG signals, their variants among subjects owing to varied types of problems encountered; it has become essential to, continuously, expand the scope of analysis to provide more and useful information from the ECG data. This warrants for a flexible architecture for ECG signal analysis. This paper presents one such flexible architecture. The authors are working towards identification of appropriate interfaces and their definitions.**

***Index Terms*—QRS detection, ECG signal analysis, parallel processing, cardiac arrhythmia.**

I. Introduction

Traditionally, clinical examinations of the human anatomy, diagnosis of problem areas, quantitative assessment and, finally, the remedial measures, were, predominantly addressed by human intellectuals with no assistance from advanced technologies. However, from the past two decades, high performance computing techniques, embedded hardware and information technology have, together, continuously, been adding potential dimensions to their initial debut in biomedical instrumentation and related domains. Electrocardiography (ECG) is one such biomedical instrumentation technology, which, by itself, is the electrical manifestation of the behavior associated with the heart. The state of cardiac health is generally reflected in the shape of the ECG waveform and heart rate [1]. An electrocardiogram can contain important pointers to the nature of diseases afflicting the heart. Owing to the non-stationary nature of the ECG signals, it is essential to acquire ECG patterns for long duration of time, analyze and conclude on any opinion. Further, the cardiovascular system is too complex to be linear, and treating it as a non-linear system can lead to better understanding of the system dynamics. Research paper by Jiapu Pan and Tompkin [2] is a landmark publication, which has addressed real time QRS detection of cardiac signals. Sun *et al.* [3] have proposed a non-linear technique for arrhythmia detection using the ECG signal. Khadra *et al.* [4] could propose mechanism to classify cardiac arrhythmias based on wavelet transforms. While Dingfie *et al*. have proposed a classification technique to classify cardiac arrhythmia into six classes using autoregressive modeling [5], R Acharya *et al*. have used Heart Rate Variability (HRV) [6] as the base signal for classification of cardiac abnormalities into eight classes.

The ECG signal analysis by itself is a complex and is evolving in terms of it enabling future strides in addressing cardiac related diagnosis. In terms of the computation time, ECG analysis is not a very time consuming process since even the, nominally, achievable sampling period is well within the maximum signal frequency that the process encounters. However, owing to the complexity and the need to provide extensibility, it may be necessary to have a flexible and extensible platform for ECG signal analysis which be extensible into ECG signal based diagnosis systems. An attempt is being made in this paper to propose a platform based on parallel processing paradigms. The implementation of such a platform is at the initial stages with the authors.

This paper is organized as follows: Section II presents briefly a typical QRS detection process. Section III presents the proposed architecture for the ECG signal based diagnosis system. Section IV draws the conclusions of this paper.

II. Typical QRS Detection Process

QRS detectors, Arrhythmia monitors (recent commercial implementation of QRS detectors) and such similar manifestations, typically, include the following functional blocks:

1) Data acquisition
2) Signal conditioning.
3) Linear digital filtering
4) Non-linear transformation
5) Decision mechanism

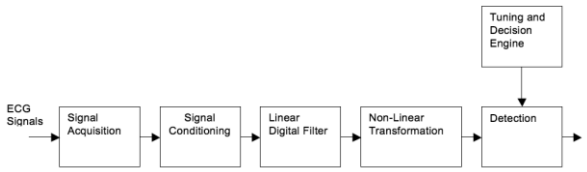

Fig. 1. Functional schematic of a typical ECG signal analysis system.

As is shown in Fig. 1, the digital filter block is, essentially, a band pass filter that is, possibly, built as a cascade of a Low Pass Filter (LPF) and a High Pass Filter (HPF). The use of band pass filter improves the Signal-to-Noise (S/N) ratio and hence enables the use of lower thresholds thus leading to improved detection sensitivity The non linear transformation is, essentially, implemented as a differentiator. Although this exercises an ideal attempt in detecting the QRS complexes, this functional block has its intrinsic impact owing to which there exists reasonable compromise on the width of the QRS complex and also its amplitude. The squaring process intensifies the slope of the frequency response curve of the

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derivative and helps restrict false positives caused by T waves with higher than usual special energies. The output of the squaring block shall be passed thro' the decision making mechanism which, effectively, detect the QRS complexes. The decision mechanism, nominally, include a sets of thresholds to be applicable, mainly, based on the input signal strength, noise immunity (internal to the system or exterior to it), etc.

III. Parallel Processing Architecture

The need for faster computation, Real Time requirements as a domain requirement (Hard Real Time Systems) and other non-critical real time needs (Soft Real Time Systems) and such similar needs have been well addressed by diversified technologies. Quest for high-speed processors, VLSI/FPGA based designs, Numeric Data Processors (NDPs), parallel architectures, model independent techniques, etc. are technologies which have attempted to provide adequate resolutions for the real time needs. Each of these technologies has a justifiably, strong binding with a specific class of applications for which their applicability can, strongly, be advocated on the techno-commercial front. As such, each of these technologies has grown into their independent discipline themselves.

Speaking in specific of the parallel processing techniques, important types of architectures are:

1) SISD / SIMD / MISD / MIMD
2) Pipe line architectures
3) Array processors
4) Shared bus / Shared memory architectures

A study of the typical ECG analyzer architecture and their possible extensions coupled with the objective of providing a flexible, extensible architecture as a scalable architecture for this scalable application, a hybrid architecture based on pipe line architecture and the array processor is conceptualized for ECG analysis. Motivations for the assumed architectural and justifications for the architectural decisions are briefed in the following paragraphs.

In reference to the existing set up, typically, employed for ECG analysis, following shows the processing time by the timing analysis approach.

TABLE I: Timing Analysis Approach

Sl.No.	Functional Block	Processing Time
1.	Signal Conditioning	T_{sc}
2.	Filter	T_{sc}
3.	Transformation	T_{trans}
4.	Detection	t_d

Assuming 300 samples per second to be adequate for the ECG signals, the time available for the functional blocks shown in Table I is 3 milliseconds (ms). With this, the average processing time available for each of the functional blocks of Table I is given as (3.0/4.0) ms. Although this throughput is achievable, easily, it suffers from the following:

1) Timing might still become a concern if each of these functional blocks grow in terms of their complexity.
2) High-speed circuits are potential source of noise. Despite the fact that these noise levels might be checked to remain within certain limits, in view of the sanctity that one attaches to bio-signals, it may not be viewed conservative if even medium speed circuits are employed as functional blocks. However, the quantitative meaning of high speed and medium speed is no standard by any means but only subjective.

In view of the above considerations, it is proposed to carry out the tasks of these functional blocks (refer Table I), by explicit low speed processors, concurrently. Using this basic idea, it is possible to build an architecture based on pipeline processing paradigm so as to achieve acceptable throughput without increasing the speed of the individual processing blocks. With this architecture, the maximum latency which any sample suffers shall be max [T_{sc}, T_{sc}, T_{trans}, T_d]. Symbolic representation of four processes (in a generic manner) is depicted in Fig. 2. It is clear that the throughput has increased with no increase in the absolute speed of any of the functional blocks. However, the overhead of this arrangement lies in the additional task of defining the proper interfaces between successive blocks. These interfaces and their definitions need be guided by the following:

1) Task complexity should have a good fitment with the available processing power
2) There shall be some left out wheeling power firstly to address any sort of exigencies and secondly to accommodate any refinement and improvisation of the tasks
3) The interface identification shall be such that it minimizes the blockage of the pipe. Any of the functional units in the pipe is capable enough to block the pipe leading to a grinding halt of the entire pipe. This is, in fact, a well-noted deficiency of the pipeline architecture, itself.

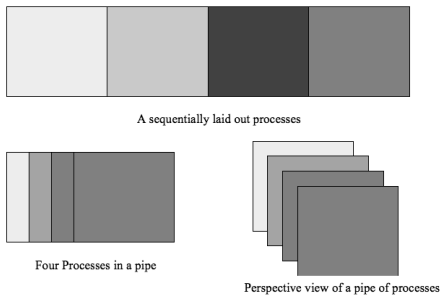

Fig. 2. Processes in a pipe line architecture.

In addition to the pipeline architecture briefed so far, this architecture also proposes an additional processor whose job shall be to compute the thresholds, selection of the thresholds, tuning parameters, decision algorithms, etc. which are required by one or more functional blocks of the pipeline. This processor block shall not, obviously, be a part of the pipe but will have interfaces with each of the units of the pipe as shown in Fig. 3.

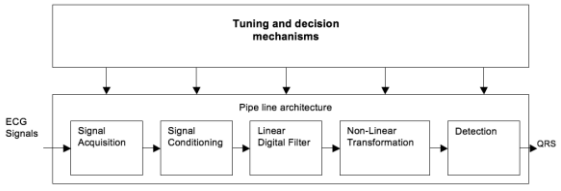

Fig. 3. Processes in hybrid architecture for ECG signal analysis.

As shown in Fig. 3, the proposed architecture is a hybrid architecture which has a pipe line architecture working concurrently with a tuning and decision mechanism processor, concurrently on an MIMD (Multiple Instruction Multiple Data) principle. At the outset, an explicit processor shall look superfluous for the scheduled activity. However, in view of the extensibility, it is essential to dedicate a processor for this activity. The authors are studying the identification of software interfaces and their definitions, for the proposed architecture.

IV. Conclusions

This paper has presented an initial work of the authors in their attempt to architect a flexible platform for ECG analysis. Whereas the technologies available for the realization of this architecture are very mature, identification of the interfaces in this architecture along with their definitions need be done very carefully to, fully, ensure extensibility of the ECG analysis, which can be scheduled on this architecture. Simultaneously, it is essential that the architecture shall be extensible by itself. The identification of the interfaces and their definitions is the ongoing activity of the authors. The authors wish to model this architecture, realize this architecture and conduct case studies on this architecture as their future research work.

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