# Design and Implementation of a Very Low Cost Surveillance System

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***Abstract*—Block truncation coding is an image compression algorithm that has lower efficiency in compare with some other algorithms, but also has low cost and complexity. FPGAs are used for implementing fast digital systems, but they have more cost. In this paper, a surveillance system is designed and implemented based on the BTC image compression algorithm using some parallel microcontrollers that has very low cost and suitable speed.**

***Index Terms*—BTC; motion detection; AVR microcontroller; division**

## I. Introduction

In many digital image systems, one image compression algorithm is used to reduce the image size to increment the use of memory. This image compression algorithm must have suitable efficiency and high speed. JPEG and JPEG2000 are examples of these compression algorithms that have high efficiency and compression ratio, but also have high complexity and cost[1],[2].

In every application, the way of hardware implementation is selected based on acceptable speed, fault tolerancy, cost and circuit size. There are two main ways to implement hardware based systems. The advent of high-density field programmable gate arrays (FPGAs), in combination with new synthesis tools, has made it relatively easy to produce programmable custom hardware[3]. Implementations on FPGAs can provide high performance within certain design constraints, demonstrating speedups of orders of magnitude over conventional machines [4]. In FPGA based systems, circuits are designed as block diagrams and connections between them. Then, by using of hardware description languages (for example, VHDL) or prepared circuit blocks, the system is implemented. FPGAs have high speed and many facilities, but because of high cost, are not acceptable in many applications. One of these implemented algorithms is block truncation coding (BTC) [5],[6]. BTC is a simple and effective technique for image compression that applies lossy compression principles [7]. Another way is microcontroller based systems that can accept instructions in their memory and execute them. One of the main problems of low cost microcontrollers is their low speed in compare with FPGAs. In some applications, using of some parallel and pipelined microcontrollers can overcome this problem.

In section II, the BTC algorithm is explained. Section III, explains the new proposed motion detection algorithm. In section IV, the system is designed using some processing units. Section V, is about the new proposed division operation in AVR microcontrollers. In section VI, the system is implemented and the speed analysis is described in section VII. Finally, section VIII, explains the conclusion.

Manuscript received May 24, 2012; revised July 19, 2012.

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## II. Block Truncation Coding

The BTC algorithm [7] divides the image into small rectangular blocks of pixels(for example, 8×8). The compression is achieved by producing a bit map for the quantized block and two 8-bits quantization levels. Increasing the block size will increase the compression ratio at the cost of reduced quality of the restored image.

For each block, the average value is calculated. A two-level quantization is performed for the entire block so that a '0' value is stored for the pixels with values smaller than the average, and the rest of the pixels are represented by the value '1'.These '0's and '1's produce the bit map of image block. Therefore, one '0' or '1' is exist in bit map instead of 8 bits in original image.

Moreover, two gray levels are produced for each block. One of them is low average that represents the average of the gray levels for the pixels whose gray level is less than the block average. The other is high average that relates to the average of the gray levels for the pixels have greater value than the block average. Therefore, for each block that have 64 pixels (64 bytes), 10 bytes are stored in the compressed version, 8 bytes that relates to the bit map of the block(one bit for every pixel) and 2 bytes that represent the block low average and block high average. As a result, the compression ratio is 6.4. In image reconstruction process, '0' is replaced by block low average and '1' is replaced by block high average.

## III. Motion Detection Algorithm

### A. Simple Motion Detection Algorithm

Some of algorithms calculate the difference between the all pixels of two continuous images and then add these differences to calculate the overall difference. If this overall difference exceeds the specified threshold, it is concluded that a motion is occurred. Calculating the difference between pixels can be stopped when the summation of differences exceed the threshold. Suppose that **m** is the number of rows and **n** is the number of columns of image. Therefore, in the worst case, the number of comparisons is m×n.

We can divide the image into blocks and calculate the summation of differences between the averages of every two blocks in the same situation of two continuous images. In this way, the number of comparisons is very smaller than the first way, but at first, the average of all blocks of the two images must be calculated. Also it is possible that the two blocks of two images have considerable difference, but the difference between their averages is not noticeable shown in Fig. 1. This is just an example and many another situations exist. Suppose that the size of blocks is 8×8, therefor, in the worst case, the number of comparisons is the same as the number of blocks in one image, namely m/8×n/8.

Fig. 1. A simple example of two related blocks in two images

### B. The proposed Motion Detection Algorithm

If we decide to use of BTC image compression algorithm to decrease the size of images containing motions, we can use the results of this compression to detecting motions that occure in the environment. We propose the new motion detection algorithm that named it BTC-MD(BTC based Motion Detection). In this method, each image is compressed using of BTC image compression and the low average and high average of any block is calculated. Then, the difference between the low averages of the same blocks of two continuous images is calculated. Also, the difference between the high averages is calculated separately. Then, the summation of all differences is calculated and compared with the threshold specified based on the environment. If the calculated summation is equal or greater than the threshold, the compressed image is saved in the memory. The stage of this method is illustrated in Fig. 2.

This method is done for each two continuous images such that ***image1*** is the current image and ***image2*** is the next image. When the process ends, image2 will be the current image and gets the image1 place. Next arrived image will be the next image as image2. The variable named ***Number*** is the number of pixels in one block. ***Counter*** specifies the index of block. This method also has some problems. For example, the two blocks of two images may have considerable difference, but the difference between their low averages and high averages is not noticeable shown in Fig. 3, but the probability of this situation is very smaller than the previous situation.

Fig. 3. Two blocks have considerable difference, but the difference between their low averages and high averages is not noticeable

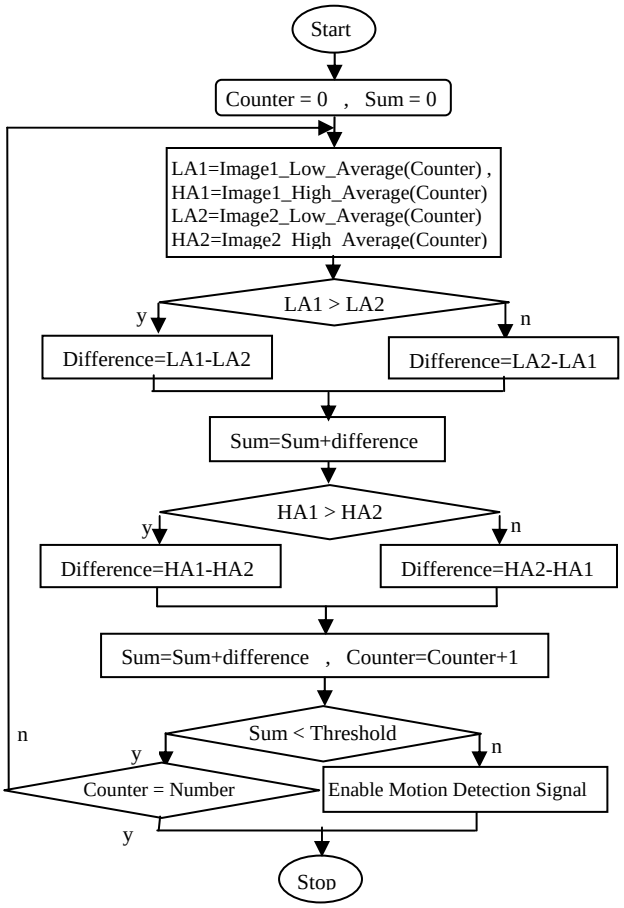


Fig. 2. The BTC-MD method

## IV. Parallel Processing

### A. Using of Parallel Microcontrollers

Suppose that there is only one block compression unit in the system. When this unit gets the pixels of one block, must process the operations and produce the bit map, block low average and block high average. Therefore, in the time of compression of this block, receiving of another block is delayed. Even if this unit can receive all blocks of this image, receiving of another image is delayed. For this reason, several processing units are used to improve the system efficiency [8]. The designed system is shown in Fig. 4.

The presented system can receive input images(for example, from a camera) consecutively. There are four compression units that act in the same way. The control unit informs four units consecutively to receive their related block with 64 bytes of data. The motion detection unit, enables the motion detection signal based on the received images. The two store units save images in the MMC memory.

### B. Operations

Compression unit 1 receives the 64 bytes of data related to block 1 and saves them in its internal SRAM memory. Simultaneously, the sum of block values is calculated. Then while the compression unit 1 operates next calculations (for example, division of block sum by 64 to produce the block average), the compression unit 2 receives the 64 bytes of block 2. Then while unit 1 operates next required operations and unit 2 finishes the receiving and starts the operations, unit

3 receives the 64 bytes of data related to block 3. Finally, while unit 1 starts to send compressed data to store unit 1, store unit 2 and motion detection unit, unit 2 operates last operations, unit 3 operates next operations and unit 4 receives the 64 bytes related to block 4. This cycle repeated again and again to receiving data with four units consecutively.

When one unit receives all data related to one block, the block sum is calculated. The sum of block must be divided by 64 to get the block average. For this operation, the sum of block is shifted to the right by 6 bits that executed very fast. Then the unit reads 64 bytes stored in internal SRAM consecutively and compare them with block average. if the pixel value is smaller than the block average, adds it to the block low sum, adds 1 to the low counter and place 0 in the bit map. Otherwise, adds it to the block high sum, adds 1 to the high counter and place 1 in the bit map. In the end of this stage, we have the sum of pixel values smaller than block average in block low sum and the sum of pixel values equal or greater than block average in block high sum. We also have the number of smaller values in low counter and the number of greater values in high counter. Low counter and high counter can have arbitrary values between 0 and 64 based on the related block. Therefore, we cannot use right shift to divide the block low sum by low counter to calculate block low average and to divide block high sum by high counter to calculate the block high average.

The number of compression units is configured in a way that no interruption take place in the operations of units and also no confusion exist in the receiving data from input and sending compressed data.

The control unit sends a signal to units 1 to 4 and informs them for receiving data from input. While one unit is receiving data, input lines of other units are in high ampedance state. Also when one unit is sending compressed data, output lines of other units are in high ampedance state.

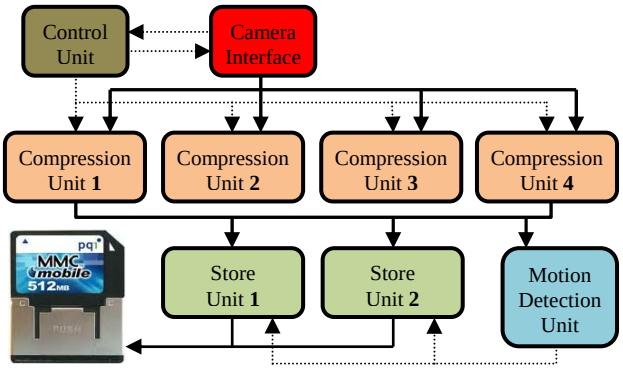


Fig. 4. the system designed for surveillance system

Compression units send bit map, block low average and block high average to the store units. Also, compression units send block low average and block high average to the motion detection unit. When the motion detection unit receives the block low and high average of two continuous images, calculates the summation of differences and compare it with the threshold. If the summation exceeds the threshold, motion detection unit inform store units to save compressed image in the MMC memory.

Each sector in the MMC memory is 512 bytes. When the store unit 1 is saving one sector in the MMC memory, store unit 2 can receive the data from compression units. we can save the compressed image in the MMC memory and when the motion detection unit enables the signal, the next compressed image is saved in a new place in the MMC, otherwise, the next compressed image is saved in the before image place. Therefore, only those images that contain motion are saved in the MMC.

## V. New Division Algorithm

We use AVR microcontrollers in the implemented system, because they have very low cost, but they cannot execute the division operation. We can use the continuous subtraction to calculate block low average and block high average, but this calculation is very time consuming. Therefore we must find another way.

We use the new division algorithm that named it hierarchical subtract based division (HSD)[8]. This new algorithm can decrement the division time and have important role to increment the number of images that can be received in one second. In HSD, initially some coefficients are selected based on the divisor that here is low counter and high counter. Because the divisor is between 0 and 64, we select 55,25,8,3 as four coefficients. We can select arbitrary coefficients but, it should be noted that the difference between them must not be small. Then, the multiplication of divisor and every coefficient are calculated. Maybe this work waste time a little, but speedups next stages. In AVR microcontrollers, the multiplication is executed in one cycle. Then, the dividend is compared with the greatest product. If the dividend is equal or greater than the greatest product, we add the greatest coefficient to the quotient and subtract the greatest product from dividend. This operation continues with comparing the decremented dividend and the greatest product again and again and when the dividend becomes smaller than the greatest product, in the next stage, the dividend is compared with the next greater product and so on. Fig. 5 shows the stages of this algorithm.

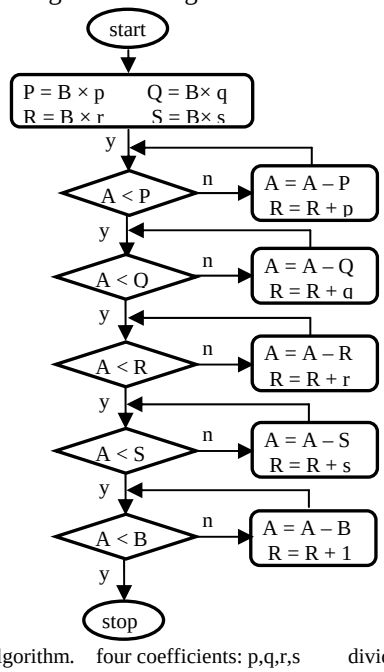


Fig. 5. HSD algorithm. four coefficients: p,q,r,s dividend:A divisor: B quotient:R four products: P,Q,R,S

If we use continuous subtraction, after every comparison and when the dividend is greater than the divisor, the quotient is incremented one unit and the number of comparisons and increments is almost equal to quotient, but if we use HSD, several comparisons and subtractions are done in one stage. For example, if the result of division (quotient) is 59, in the first stage, 55 is added to quotient and in the second stage, 3 is added to the quotient. Therefore, the processing that is done in two stages is equal to 58 stages in continuous subtraction. In the final stage, dividend is compared with the divisor and 1 added to the quotient and the result is 59.

## VI. System Implementation

### A. Microcontrollers and Connections

In this sysem, we use one ATmega 8 for control unit and seven Atmega 32 for other units. Pin configuration of these microcontrollers is shown in Fig. 6.

When the data ready line that is connected to portc pin 0 of control unit, becomes high, control unit informs one of the compression units to receive 8 bit data related to one pixel of image block. When control unit informs one unit for 64 times to receive 64 bytes, in the next stage, informs another unit to receive 64 bytes and so on. At first, compression unit 1 is busy. Then, compression units 1 and 2 are busy for different stages of compression algorithm. This process continues until compression unit 4 starts to receive data. In this time and until the system is on, all units are busy and therefore, only at small time in the system start, maximum use of units is not possible.

### B. MMC memory

We decided to save compressed images in MMC memory that requires 3.3 volts to work, while AVR microcontrollers require 5 volts. The data must be sent from output port of microcontrollers to MMC, has 5 volts and must be decremented to 3.3 volts to connect to MMC input lines. This problem is solved by resistant network that is shown in Fig. 6.

AVR microcontrollers have the SPI interface and can connect to the MMC memory. Microcontroller is master and the MMC memory is slave. Four lines are required for SPI connection as shown in Fig. 6.

The implemented system is shown in Fig. 7. It should be noted that the large size of circuit is because of using the microcontrollers in the PDIP package and placing the system in the 1000 holes board. If we use the microcontrollers in the TQFP package and place them on the printed circuit board, the circuit size will be very small.

## VII. Speed Calculation

In the implemented system, the maximum frequency (16MHZ) is used for microcontrollers via external oscillator. All instructions are written in assembly language using AVR Studio Synthesis tool.

The number of required cycles for any instruction is obvious. Our calculation shows that receiving 64 bytes of data related to one block takes 1040 cycles. In each second, 16 million cycles exist and therefore 15384 blocks can be received in one second. We test the system with 256×256 images that have 1024 blocks. If we divide the number of received blocks in a second by 1024, the speed of 15 images per second can be achieved that is practically observable.

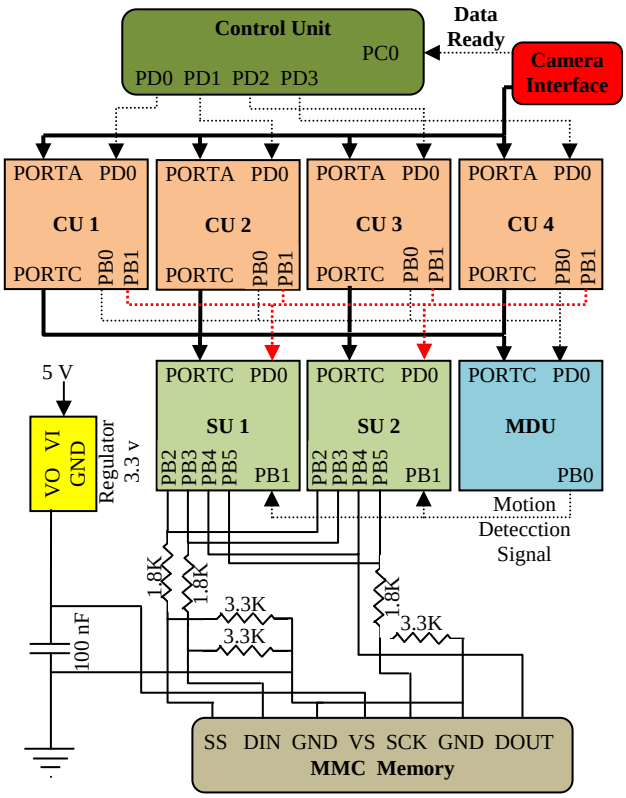


Fig. 6. Pin configuration of microcontrollers
CU:compression unit SU:store unit MDU:motion detection unit

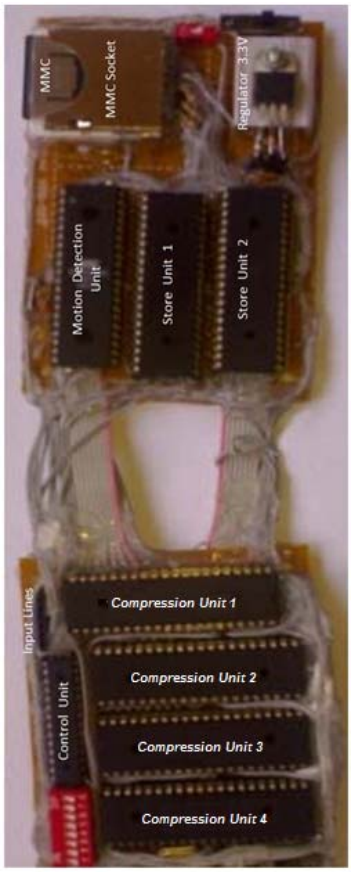


Fig. 7. The implemented system

## VIII. Conclusion

As shown in this paper, we can use several parallel microcontrollers and divide jobs between them to create different systems with acceptable speed and very low cost that can be used instead of expensive FPGAs in applications that the time of processing is not very critical. As mentioned before, parallelism have been done in both main segments, i.e. motion detection with store and compression segments, therefore, the cost of the system is incremented a little, but noticeable efficiency can be achieved.

## Acknowledgment

This paper is a result of the research plan "Design a hardware system for the JPEG2000 image compression algorithm". In fact, while working on this research plan, we decided to use some parallel AVR microcontrollers to have suitable speed and very low cost. At first, we used this approach for the simpler image compression algorithm "BTC" and motion detection to test our way.

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