MCDC: A Novel Mixed Clock Deskewing Circuit

Rong Ji, Bin Tian, Wenhui Cui, Jiang Shi, Zhenyu Sun, and Zhaoqiang Yang

***Abstract*—In modern synchronous digital systems, the clock skew problem becomes one of the bottlenecks in achieving high speed and high performance. Several clock deskewing circuits have been used to reduce clock skew. The synchronous mirror delay (SMD) and the delay-locked loop (DLL) are two typical kinds of them. SMDs have advantages of short locking time and low-power characteristics within a wide compensation range, but coarse deskewing resolution are inherent shortcoming of them. Reversely, DLLs have the high deskewing resolution, but long locking time and high power within a wide compensation range are immanent disadvantages of them. Thus, a novel mixed clock deskewing circuit (MCDC), which is mostly a SMD structure with a DLL technique in support, is presented in this paper. The proposed MCDC takes advantages in the other part and complements its weak points each other. The simulation results show that the MCDC has advantages of high resolution, fast locking and low power. In addition, it has a small area characteristic which is propitious to be integrated into high-performance microprocessors.**

***Index Terms*—Clock skew, deskewing circuit, delay-locked loop, synchronous mirror delay.**

I. Introduction

With the rapid advances in deep-submicron CMOS processes, modern digital systems have been successfully operated at GHz for many years, such as high-speed data links, multiprocessor systems, and so forth. The clock skew problem becomes one of the bottlenecks in realizing high speed and high performance digital systems [1].

Clock deskewing circuit techniques have been used to reduce clock skew. SMDs and the DLLs are two typical species of clock deskewing circuit techniques. Although SMDs have advantages of short locking time and low-power characteristics within a wide compensation range, coarse deskewing resolution are inherent shortcoming of them [2], [3]. Reversely, DLLs have the high deskewing resolution, but long locking time and high power within a wide compensation range are immanent disadvantages of them [4], [5].

Thus, MCDC, a novel mixed clock deskewing circuit combining SMDs with DLLs together, which take advantages in the other part and complements its weak points each other, is proposed. The proposed mixed clock deskewing circuit adopts a mixed clock skew compensation technique which is mostly the SMD circuit techniques and with the DLL techniques in support to achieve fast-locking, low-power, and high-resolution performances of the deskewing circuit.

The rest of this paper is organized as follows. Section II describes the design concept and the architecture of the proposed MCDC. Section III describes the design details of the main components of the MCDC. Section IV presents the simulation results of the MCDC. Finally, conclusions are given in Section V.

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II. Architecture of the Proposed MCDC

The proposed MCDC architecture consists of a coarse compensation module and a fine compensation module. The coarse compensation module is fulfilled by the novel SMD circuit. The SMD coarse compensation module can compensate quickly the large-scale clock skew of the input clock signal and make the clock skew equal to or smaller than unit delay size within three clock cycles. In order to ensure high deskewing resolution, the fine compensation module achieved by the digital DLL is used. The DLL fine compensation module is embedded in the SMD circuit to remove the residual skew less than the unit delay of the SMD. As shown in Fig. 1, for the sake of short locking time and saving power, the digital DLL fine compensation module is only embedded in the second delay unit of the measure delay line and the last but one delay unit of the variable delay line in the SMD coarse compensation module.

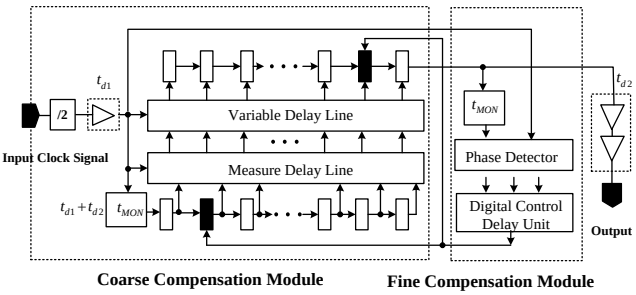

Fig. 1. Architecture of the proposed MCDC.

III. Circuit Design of the MCDC

A. SMD Coarse Compensation Module

The SMD coarse compensation module is used to align quickly the phase of the internal clock to that of the external clock. The SMD measures the cycle time of the input clock signal by a measure delay line, and controls the propagation path of variable delay line to achieve clock skew compensation of the input clock signal. As shown in Fig. 1, the SMD coarse compensation module consists of a frequency-halving divider which is adopted to avoid the conflict between the RESET signal and the measure start time in the measure delay line and guarantee ±50% clock

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deskewing range, the clock input buffer whose delay is t_{d1}, the clock driver whose delay is t_{d2}, the mirror delay t_{MON} (t_{MON} = t_{d1} +t_{d2}), a measure delay line, and a variable delay line.

In the SMD coarse compensation module, the measure delay line and the variable delay line are key components.

1) The measure delay line

The architecture diagram of the measure delay line is shown in Fig. 2. Each delay cell consists of a basic delay cell and a sampling circuit. As shown in Fig. 3, the basic delay cell and the sampling circuit are implemented by a two-input NAND gate and a C^2MOS circuit respectively. The initial input to the delay line is set high. When the CLK signal is high, the measure delay line starts the measurement of time delay. The reset pulse signal RESET is set high during the CLK signal being low. Therefore, the propagation and the sampling of signal "1" can be made by turns. When the RESET signal and the CLK signal are low simultaneously, the sampling circuit will start to sample the OUT signal which is the output of the delay cell, and the sampling result Q is transmitted to the control port of the variable delay line. When the RESET signal is high, the sampling circuit will turn off and wait for CLK being set high to begin a new round of delay measure operation.

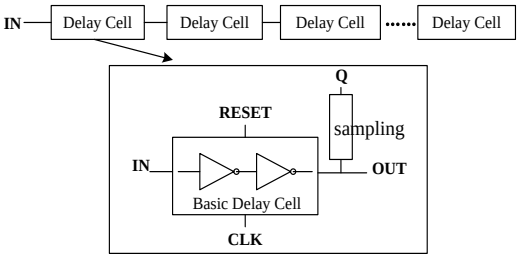

Fig. 2. Circuit diagram of the measure delay line.

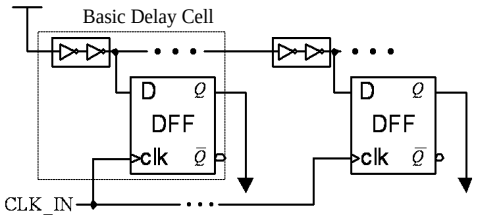

Fig. 3. Schematic of the basic delay cell.

Furthermore, in the design of the measure delay line, in order to improve the sampling resolution, a novel integrative circuit of delay sampling, which can completely conceal the setup time of the D-flip flops (DFFs), is designed to avoid the impact of the D-flip flop setup time upon the sampling accuracy. The diagram of the integrative circuit is shown in Fig. 4. In the integrative circuit, the NAND logic is embedded in the master latch. When the CLK signal and the RESET signal are high simultaneously, the master latch is equivalent to 2-level cascading NAND gates. When the CLK signal is low, the master latch is in the hold state, and the sampling information of the slave latch will represent the situation of the IN signal propagating in the 2-level cascading NAND gates. That is equivalent to zero setup time. In the design of the measure delay, all basic delay cells with the exception of the second basic delay cell adopt this delay sampling integrative circuit.

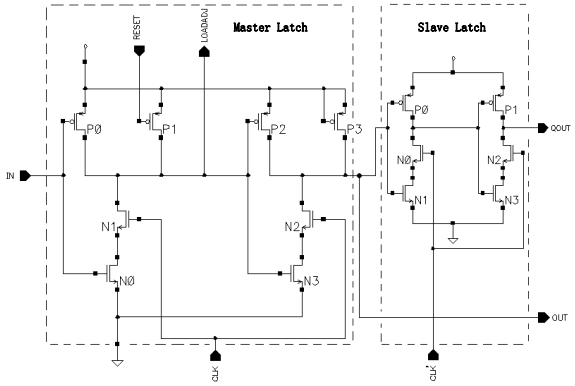

Fig. 4. Delay Sampling Integration Circuit.

For the second basic delay cell of the measure delay line, it adopts a special delay sampling integrative circuit, in which the digital control delay unit of the DLL fine compensation module is embedded between P1 and P2 in Fig. 4.

2) The variable delay line

In the variable delay line, a novel delay path selection circuit without clock tree is designed to reduce the power dissipation of the deskewing circuit. The architecture of the variable delay line circuit is shown in Fig. 5. The variable delay line is composed of cascading NAND gates, and has a mirror symmetric structure with the measure delay line. In Fig. 5, the fine delay unit is the digital control delay unit of the DLL fine compensation module.

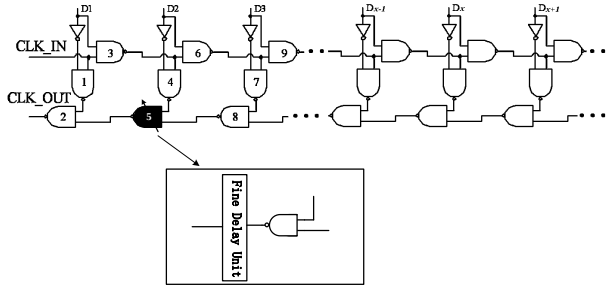

Fig. 5. Schematic of the variable delay circuit.

In order to guarantee the high accuracy of delay results, the sizes of all NAND gates in the variable delay line circuit are same, and equal to the sizes of all delay cells in the measure delay line. $D_1, D_2, \ldots D_n$ are the control ports of the delay path, which are corresponding to every measure delay cell in the measure delay line. If all control ports are zero, the input clock will reach the output port of the variable delay line through the first and second NAND gates. In this case, the loop delay t_{delay} is

$$t_{delay} = t_{delay1} + t_{delay2} = 2t_{nand\_delay} \quad (1)$$

In (1), t_{nand_delay} is the delay of NAND gate, t_{delay1} and t_{delay2} are the delay of the first NAND and the second NAND gate respectively. If D_1 is '1' and D_2 is '0', the sampling results of the measure delay line Q_1 and Q_2 will be '1' and '0', respectively. It means that the current high level propagating stops at the first delay cell in the measure delay line, the input clock will only propagate along the third, the fourth, the fifths, and the second NAND gate to the output port of the variable

delay line. In this instance, the loop delay is

$$t_{delay} = t_{delay3} + t_{delay4} + t_{delay5} + t_{delay2} = 4t_{nand\_delay} \quad (2)$$

In (2), t_{delay2}, t_{delay3}, t_{delay4} and t_{delay5} are the delay of the second, third, fourth and fifth NAND gate, respectively. Similarly, when $D_1D_2\ldots D_{x-1}D_xD_{x+1}=11\ldots110$, the total delay of CLK_IN is $2(x+1)t_{NAND}$.

B. DLL Fine Compensation Module

The fine compensation module is used to eliminate remainder clock skew which has been compensated by SMD. For low power and fast locking, the fine delay module is only embedded in two basic delay cells in the coarse compensation module. One is the second basic delay cell in the measure delay line. Another is the last but one basic delay cell in the variable delay line. The architecture of the fine compensation module is shown in Fig. 6. In the DLL fine compensation module, the phase detector and the digital control delay unit are key components.

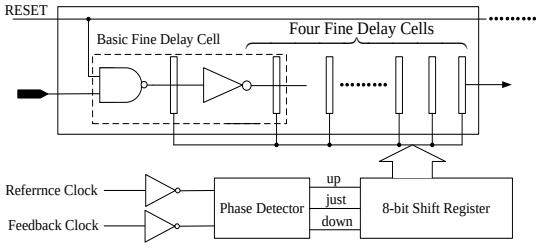

Fig. 6. Architecture of the DLL fine compensation module.

1) The phase detector

The phase detector is used to achieve the phase comparison between the feedback clock to be compensated and the standard reference clock. Circuit logic diagram of the phase detector in the fine compensation module is shown in Fig. 7.

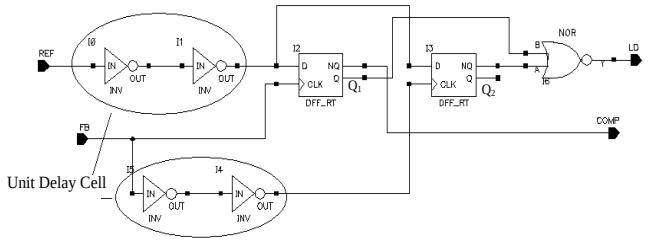

Fig. 7. Circuit logic of the phase detector.

In Fig. 7, REF is the input port of the standard reference clock. FB is the input port of feedback clock to be compensated. A two-level inverter is a unit delay cell. Unit delay cells play two roles in the phase detector. One role is to postpone the standard reference clock delayed for a unit delay. Another role is to separate the reference clock from the rear level load to reduce the reference clock's skew. The reference clock signal postponed for a unit delay is sampled by two D-type triggers respectively. One D-type trigger is triggered by the feedback signal without delay, and its sampling result is Q_1. Another D-type trigger is triggered by the feedback signal with a unit delay, and its sampling result is Q_2. LD and COMP are the compare output results between REF and FB. According to the value of Q_1 and Q_2, the logic expression of LD and COMP are

$$COMP = \overline{Q_1} \quad (3)$$

$$LD = \overline{Q_1 + \overline{Q_2}} \quad (4)$$

2) The digital control fine delay cell

The digital control fine delay cell is used to control the delay time by increasing/decreasing the amount of capacitance. The circuit logic of the digital control fine delay cell in the fine compensation module is shown in Fig. 8.

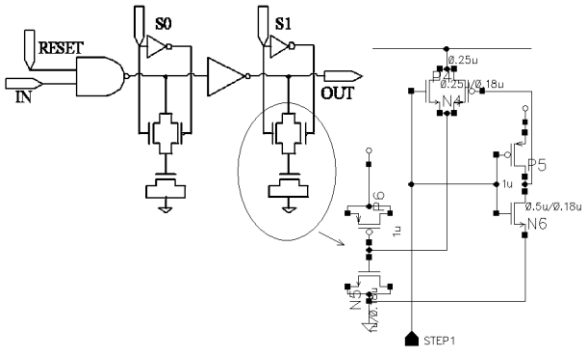

Fig. 8. Digital control fine delay cell circuit.

IV. The Simulation Results

In order to verify the circuit performance and deskewing resolution, the MCDC was designed using a 0.18μm CMOS technology with the supply voltage of 1.8V. The layout of the MCDC is shown in Fig. 9.

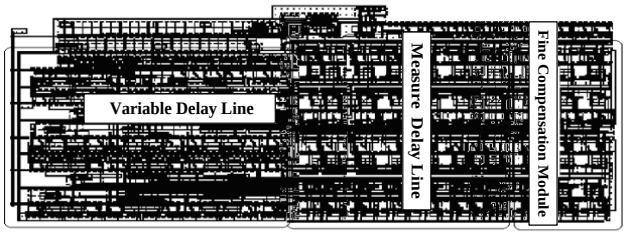

Fig. 9. Layout of the MCDC.

Moreover, some performance parameters are obtained by the SPICE post-layout simulation of the MCDC in order to compare the MCDC with some existing high-resolution clock skew compensation circuits. The performance summary of the MCDC and comparison is listed in Table I. The results show that the proposed MCDC has high-resolution and small active area characteristics. Furthermore, the MCDC has faster locking time and smaller power dissipation than [6], [7].

TABLE I: The Arrangement of Channels

	REF[6]	REF[7]	This Work
Technology	0.18μm	0.18μm	0.18μm
Supply	1.8V	1.8V	1.8V
Operating Frequency	510MHz~1100MHz	200MHz~400MHz	100MHz~1GHz
Jitter(pk-pk)	20.4ps@800MHz	23.6ps@300MHz	20ps
Lock time	< 80 cycles	≥ 6 cycles	≤ 13 cycles
Power	12mW	31.5mW(@300MHz)	9.7mW(@1GHz)
Active Area	0.0161mm^2	0.139mm^2	0.026mm^2

V. Conclusion

In this paper, we present a novel mixed deskewing circuit, which combines SMD circuit techniques with DLL circuit techniques. The proposed MCDC not only effectively avoids the shortcoming of high power dissipation and long locking time with pure DLLs, but also averts the disadvantage of low deskewing resolution with pure SMDs. It has advantages of high resolution, fast locking and low power at the same time. In addition, it has an advantage of a small area characteristic which is propitious to be integrated into high-performance microprocessors.

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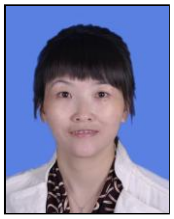

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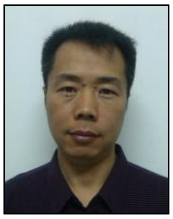

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